# IC emulates many types of logic gates

(25)

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Normally, you'd use a 4053-type triple-spdt analog switch (also called a triple, 2-channel analog multiplexer/demultiplexer) for analog signal-switching applications. When properly connected, however, the CMOS device can also emulate a variety of simple gates and flip-flops. What's more, you can save space with a 4053 by packing three types of simple logic gates into one DIP.

**Fig 1**, for example, shows the 4053's implementations and truth tables for eight logic functions. The inverter, buffers, and gates use one spdt section each; the flip-flops use two sections each. Note that the buffers are bidirectional because the 4053's input-to-output path is a symmetrical transmission gate. Also, unlike conventional buffers, they have an output impedance (on-resistance) of several hundred ohms.

In **Fig 2**, the 2-input gates require the complement of one input; if the complement isn't available, though, you can generate it using a ⅓4053 as an inverter. The circuits of **Fig 1** and **Fig 2** will work with the $V_{EE}$ terminal connected either to ground or to a negative supply voltage, provided that the 4053 and the external logic are operating from the same $V_{DD}$ and $V_{SS}$ supply levels. *(Ed Note: The 4053 requires supply voltages ($V_{DD}$ and $V_{SS}$, pins 16 and 8), plus a bias supply ($V_{EE}$, pin 7).)*

The level-shifting circuits of **Fig 3** shift the $A_{IN}$ signal

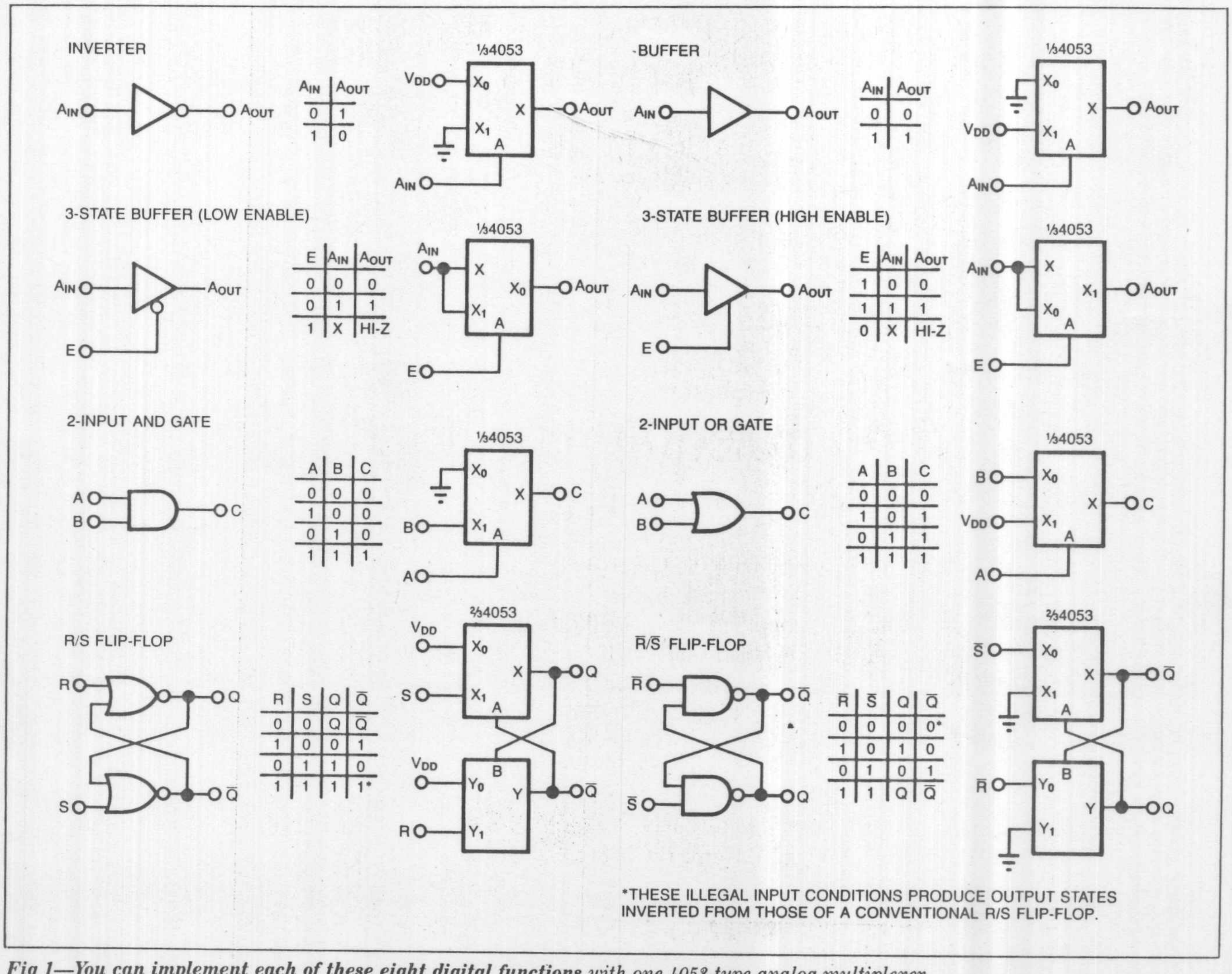


*Fig 1—You can implement each of these eight digital functions with one 4053-type analog multiplexer.*

from $V_{SS}$-$V_{DD}$ levels to $V_{EE}$-$V_{SS}$ or $V_{EE}$-$V_{DD}$ levels. $V_{EE}$ must connect to a negative supply voltage in these circuits.

In these applications, the 4053's inhibit input (pin 6) must connect to $V_{SS}$. Also, the response of the 4053-based circuits is generally slower than that of equivalent CMOS digital gates. Even though the 4053's propagation delay from switch input to switch output is faster—about one-fifth that of a CMOS gate—the delay from a 4053 control input is approximately twice that from a CMOS-gate control input. **EDN**

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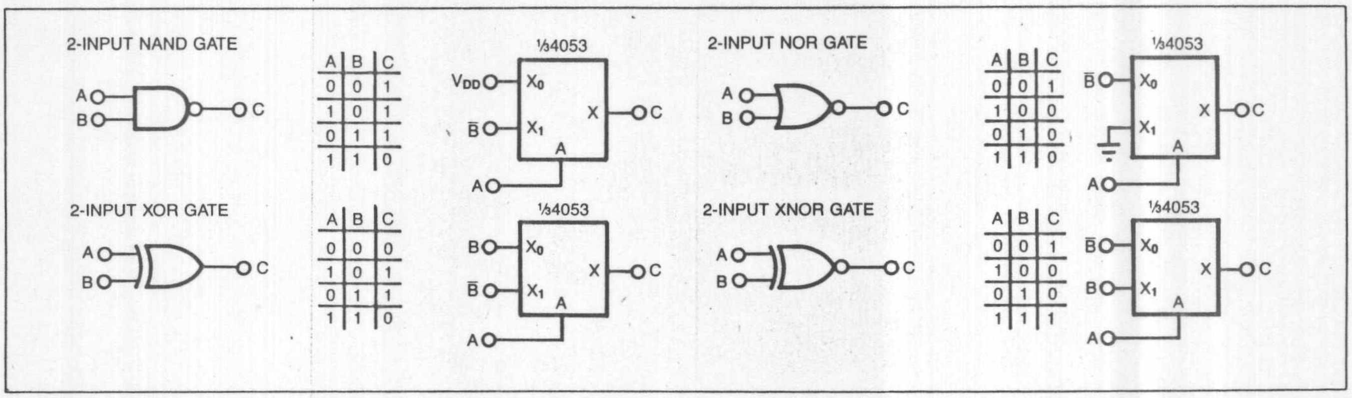


*Fig 2—**Each of these 2-input gates** requires the complement of one input if you're going to use a 4053 to effect them.*

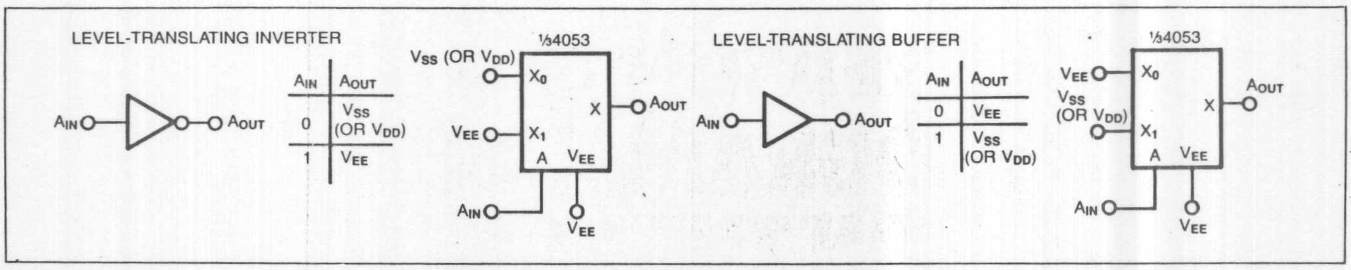


*Fig 3—**These circuits use a 4053 to translate** positive logic levels to negative logic levels (using $V_{SS}$) and to bipolar logic levels (using $V_{DD}$).*

# Digital-delay circuit is programmable

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The circuit shown in **Fig 1** lets you delay the positive digital transitions applied at the Start Input according to a programmable time interval. Within the available range, you can program a desired delay time to 16-bit accuracy.

The clock-synchronizer section synchronizes the main clock signal, 1× Clock, with the Start Input signal. When the Start Input goes from a low to a high level, the divide-by-16 counter ($IC_3$) first resets to zero, then counts at the 16× Clock rate. In the counter section, two cascaded 8-bit counters, $IC_7$ and $IC_8$, form a 16-bit counter. Because each of these ICs contains an 8-bit parallel-input register, you can store the low and high bytes of the desired delay factor by applying data at $D_0$-$D_7$ and strobing the appropriate $\overline{\text{Load}}$ input. The counters remain inactive as long as $IC_{6B}$'s Q output holds the counter's $\overline{\text{CLoad}}$ inputs high.

When a positive transition at the Start Input causes $IC_{6B}$'s Q output to go low, the 16-bit delay data passes internally from the registers to the counters. The counters immediately begin counting up from their preloaded values at the 1× Clock rate. The delayed positive-output transition occurs at pin 9 ($\overline{\text{RCO}}$) when $IC_8$'s counter rolls over from 255 to 0. Finally, $IC_{6B}$'s Q output goes high, which returns $IC_7$ and $IC_8$ to the load

state to wait for the next positive transition at the Start Input.

Delay time, $t_D$, from the Start Input signal to the Delayed-Transition Output is

$$t_D=16(65{,}535-256x-y)t_C+18.5t_C\pm0.5t_C,$$

where

$x$=the decimal value of the high-order delay byte ($0\leq x\leq255$)

$y$=the decimal value of the low-order delay byte ($0\leq y\leq255$)

$t_C$=the period of the 16× Clock signal.

To increase the maximum delay time, you can either slow down the 16× Clock (sacrificing accuracy) or add 74LS592 counters. **EDN**

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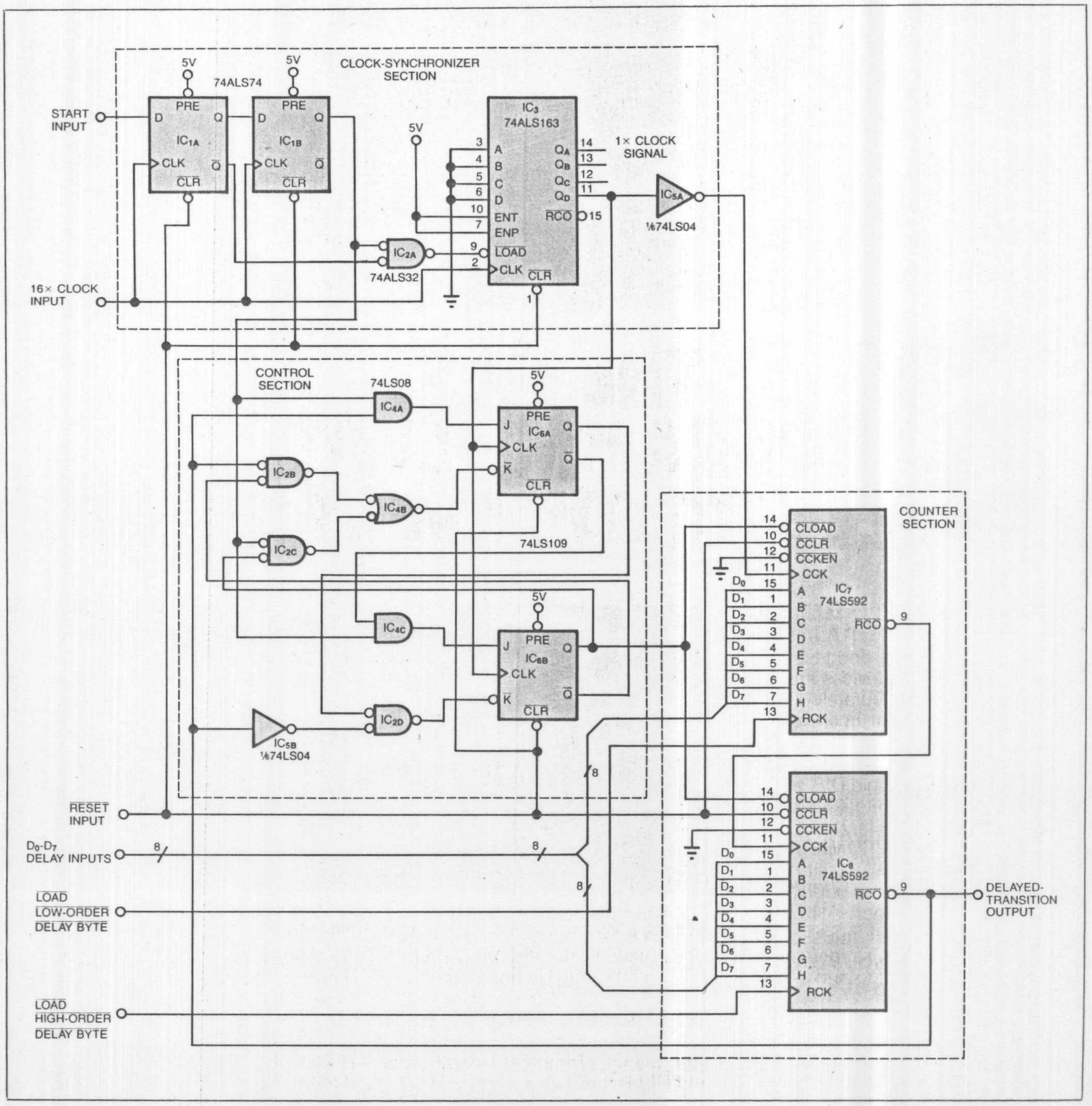


*Fig 1—**This circuit provides a programmable delay** for positive transitions at the Start Input signal. You load the 16-bit delay factor in two consecutive bytes, from the $D_0$-$D_7$ inputs.*